IN THE CLAIMS

Please cancel claims 4-5, 11-12, and 18-19 without prejudice.

Please amend claims 1, 3, 6-8, 13-15, 20-21, and 29-32 as indicated below.

1. (Currently Amended) An apparatus, comprising:

an array of tag address storage locations; and

a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache located on a memory module via a plurality of command lines and address lines over an interconnect ~~a memory bus~~, the command sequencer and serializer unit to cause a current line of data to be read out from a first location of a memory module memory device and to load a next line of data from a second location of the memory module memory device to the data cache, in response to a single command having a plurality of segments serialized and sequentially transmitted via the plurality of address lines and command lines over the interconnect ~~memory bus~~ within a single memory access transaction,

wherein the single command includes at least one of memory module destination information, cache way information, address strobe state information, cache hit information, column address information, and memory device bank information,

wherein the single command is delivered over a plurality of transfer periods within a single memory access transaction, and wherein the cache hit information and

cache way information is transferred during a last transfer period of the transfer periods.

2. (Canceled)

3. (Currently Amended) The apparatus of claim 1, wherein the single command comprises a read and preload command delivered to the data cache located on the memory module, the read and preload command to cause the current line of data to be read out from the first location of the memory module memory device and to load the next line of data from the second location of the memory module memory device to the data cache.

4. – 5. (Canceled)

6. (Currently Amended) The apparatus of claim [[5]] 3, wherein the read and preload command information is delivered over four transfer periods within a single memory access transaction.

7. (Currently Amended) ~~The apparatus of claim 6,~~

An apparatus, comprising:

an array of tag address storage locations; and

a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache located on a memory module via a plurality of command lines and address lines over an interconnect, the command sequencer and serializer unit to cause

a current line of data to be read out from a first location of a memory module memory device and to load a next line of data from a second location of the memory module memory device to the data cache, in response to a single command having a plurality of segments serialized and sequentially transmitted via the plurality of address lines and command lines over the interconnect within a single memory access transaction,

wherein the single command comprises a read and preload command delivered to the data cache located on the memory module, the read and preload command to cause the current line of data to be read out from the first location of the memory module memory device and to load the next line of data from the second location of the memory module memory device to the data cache,

wherein the read and preload command includes memory module destination information, cache way information, address strobe state information, cache hit information, column address information, and memory device bank information,

wherein the read and preload command information is delivered over four transfer periods within a single memory access transaction, and wherein the cache hit information and cache way information is transferred during the fourth transfer period of the four transfer periods.

8. (Currently Amended) A memory module, comprising:

at least one memory device; and

a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by a memory controller over a plurality of command

lines and address lines of an interconnect ~~a memory bus~~, the memory controller component including an array of tag address storage locations, the plurality of commands including a read and preload command, as a single command having a plurality of segments, when serialized and sequentially received from the memory controller over the plurality of command and address lines within a single memory access transaction, to cause a current line of data to be read out from a first location of the memory device and to load a next line of data from a second location of the memory device to the data cache,

wherein the read and preload command includes at least one of memory module destination information, cache way information, address strobe state information, cache hit information, column address information, and memory device bank information,

wherein the read and preload command is delivered over a plurality of transfer periods within a single memory access transaction, and wherein the cache hit information and cache way information is transferred during a last transfer period of the transfer periods.

9. – 12. (Canceled)

13. (Currently Amended) The memory module of claim [[12]] 8, wherein the read and preload command information is received over four transfer periods.

14. (Currently Amended) ~~The memory module of claim 13,~~

A memory module, comprising:

at least one memory device; and

a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by a memory controller over a plurality of command lines and address lines of an interconnect, the memory controller component including an array of tag address storage locations, the plurality of commands including a read and preload command, as a single command having a plurality of segments, when serialized and sequentially received from the memory controller over the plurality of command and address lines within a single memory access transaction, to cause a current line of data to be read out from a first location of the memory device and to load a next line of data from a second location of the memory device to the data cache,

wherein the read and preload command includes memory module destination information, cache way information, address strobe state information, cache hit information, column address information, and memory device bank information,

wherein the read and preload command information is received over four transfer periods, and wherein the cache hit information and cache way information is transferred during the fourth transfer period of the four transfer periods.

15. (Currently Amended) A system, comprising:

a processor;

a memory controller coupled to the processor, the memory controller including an array of tag address storage locations, and

a command sequencer and serializer unit coupled to the array of tag address storage locations; and

a memory module coupled to the memory controller via a plurality of command lines and address lines over an interconnect ~~a memory bus~~, the memory module including

at least one memory device, and

a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, one of the plurality of commands including a read and preload command, as a single command having a plurality of segments, when serialized and sequentially received from the memory controller over the plurality of command and address lines within a single memory access transaction, to cause a current line of data to be read out from a first location of the memory device and to load a next line of data from a second location of the memory device to the data cache,

wherein the read and preload command includes at least one of memory module destination information, cache way information, address strobe state information, cache hit information, column address information, and memory device bank information,

wherein the read and preload command is delivered over a plurality of transfer periods within a single memory access transaction, and wherein the cache hit information and cache way information is transferred during a last transfer period of the transfer periods.

16. (Previously Presented) The system of claim 15, wherein the memory module further includes a command decoder and deserializer unit to receive command and address information from the memory controller, the command decoder and deserializer unit providing control for the data cache.

17. – 19. (Canceled)

20. (Currently Amended) The system of claim [[19]] 15, wherein the read and preload command information is delivered over four transfer periods.

21. (Currently Amended) ~~The system of claim 20,~~

A system, comprising:

a processor;

a memory controller coupled to the processor, the memory controller including

an array of tag address storage locations, and

a command sequencer and serializer unit coupled to the array of tag address storage locations; and

a memory module coupled to the memory controller via a plurality of command lines and address lines over an interconnect, the memory module including

at least one memory device, and

a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, one of the plurality of commands including a read and preload command, as a single command having a plurality of segments, when serialized and sequentially received from

the memory controller over the plurality of command and address lines within a single memory access transaction, to cause a current line of data to be read out from a first location of the memory device and to load a next line of data from a second location of the memory device to the data cache,

wherein the memory module further includes a command decoder and deserializer unit to receive command and address information from the memory controller, the command decoder and deserializer unit providing control for the data cache,

wherein the read and preload command includes memory module destination information, cache way information, address strobe state information, cache hit information, column address information, and memory device bank information,

wherein the read and preload command information is delivered over four transfer periods, and wherein the cache hit information and cache way information is delivered during the fourth transfer period.

22. (Previously Presented) The system of claim 15, further comprising a point-to-point interconnect to couple the memory controller to the memory module.

23. – 27. (Canceled)

28. (Previously Presented) The apparatus of claim 1, wherein each of the segments is transmitted within one of the transfer periods over one of the command and address lines.

29. (Currently Amended) The apparatus of claim 28, wherein a segment of the command transmitted in [[a]] the last transfer period of a command line includes information indicating a cache hit.

30. (Currently Amended) The apparatus of claim 28, wherein a segment of the command transmitted in [[a]] the last transfer period of a command line includes information implicating a cache way of the data cache on a memory module.

31. (Currently Amended) The apparatus of claim 28, wherein a segment of the command transmitted in [[a]] the last transfer period of a command line includes eviction information of an eviction buffer of the data cache.

32. (Currently Amended) ~~The apparatus of claim 28,~~

An apparatus, comprising:

an array of tag address storage locations; and

a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache located on a memory module via a plurality of command lines and address lines over an interconnect, the command sequencer and serializer unit to cause a current line of data to be read out from a first location of a memory module memory device and to load a next line of data from a second location of the memory module memory device to the data cache, in response to a single command having a plurality of segments serialized and sequentially

transmitted via the plurality of address lines and command lines over the interconnect within a single memory access transaction,

wherein each of the segments is transmitted within one of the transfer periods over one of the command and address lines, and

wherein the plurality of transfer periods includes at least four transfer periods and wherein the plurality of command and address lines includes at least four command lines and five address lines.

33. (Previously Presented) The apparatus of claim 32, wherein a segment of the command transmitted over the first and second command lines of the four command lines during the first transfer period of the four transfer periods includes destination information indicating which memory module is being addressed.

34. (Previously Presented) The apparatus of claim 32, wherein a segment of the command transmitted over the first command line of the four command lines during the second transfer period of the four transfer periods includes state information of a row address strobe (RAS).

35. (Previously Presented) The apparatus of claim 32, wherein a segment of the command transmitted over the second command line of the four command lines during the second transfer period of the four transfer periods includes state information of a column address strobe (CAS).

36. (Previously Presented) The apparatus of claim 32, wherein a segment of the command transmitted over the third command line of the four command lines during the second transfer period of the four transfer periods includes state information of a write enable (WE) signal.